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IMPLEMENTATION AND ANALYSIS OF 6T 1BIT FULL ADDER USING CADENCE VIRTUOSO

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ABSTRACT

Many digital circuits consists adders and these adders plays a crucial role in implementation of different logic circuits. There is an urge to make the electronic devices smaller in size as much as possible. This paper presents the implementation of a 6T 1bit full adder. The circuit is simulated using Cadence virtuoso tool at 180nm technology with a supply voltage of 1.8V .The logic used is transmission function logic. Comparison of conventional 28T full adder is done with the implemented 6T full adder in terms of parameters like average power, delay, power delay product and area.

Keywords: Conventional, Simulation, Nano Meter Technology, Transmission Function Logic, Cadence Virtuoso.

I. INTRODUCTION

In Low power VLSI the primary design constraint is power consumption. Low power design plays an important role in high performance systems, as excessive power dissipation decreases the reliability and cost increases the expenditure in setting up the cooling system. Full adder is a basic building block of on chip libraries. It is a combinational circuit and finds applications in various digital circuits. These are used in processors, ALU and other computing devices. As a part of processors these are also used in calculating address, table indices etc. It adds two binary 1 bit digits along with carry in and produces sum and carryout.

II. METHODOLOGY

Previous works on full adder shows that a conventional full adder circuit implemented in CMOS technology uses 46T according to the expression

Sum=A⊕B⊕Cin i.e

Sum=A'BCin'+AB'Cin'+ABCin+A'B'Cin and

Carry=AB+BCin+CinA

By manipulating the Boolean expressions the transistors count has reduced i.e the carry out expression is manipulated as

Cout=AB+BCin+CinA => Cout=AB+Cin(A+B)

The sum expression is written in terms of Cout'(Cout bar) as,

Sum=ABCin+Cout'(A+B+Cin)

This results in full adder design with 28T. Various logics are used to reduce the transistor count followed by power consumption. Some of those techniques are Transmission Gate Logic, Domino Logic, Pass Transistor Logic, Gate Diffused Input etc. When TGI is used the count has reduced to 20T.

III. CIRCUIT IMPLEMENTATION

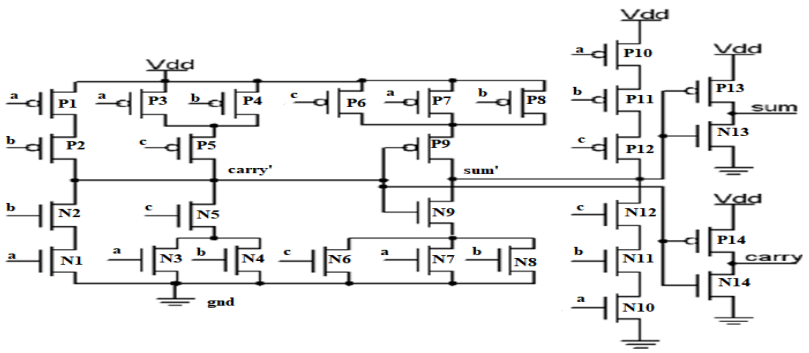

Figure 1: 28T Full Adder circuit

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CIRCUIT WORKING:

- When a=1,b=0,c=1(P2,P4 is ON & P5,P3,P1 OFF and N1, N3,N5 are ON & N2,N4 OFF).
- So, Cout' =0(as no voltage pass through P-junction) For same input P7, P6 are OFF ,P8 ,P9 are(as Cout' is zero) ON.N6, N7are ON & N8, N9 are OFF.
- So, SUM'=1(as Vdd will be connected and no connection through ground).
- Again for same input, P10, P12 are OFF and P11 is ON.N10,N12 are ON and N11 is OFF.)
- So, both path are OFF(Vdd and ground are not connected) and that's why output of this will be same as SUM'.As SUM'=1 so,N13 is ON,P13 is OFF. So, output of this is connected to ground. As a result, Sum=0.
- As Cout'=0, P14 is ON, N14 is OFF. So, Carry (output) of this is connected to Vdd and thus Carry=1.

Demerits of Using CMOS (28T):

- Due to high number of transistors, its power consumption is high.
- Large PMOS transistor in pull up network results in high input capacitances, which cause high delay and dynamic power.
- Large chip area and high input data i.e. large transistor count.

TRANSMISSION FUNCTION LOGIC

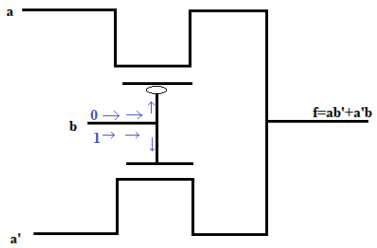

Figure 2: Transmission function logic

Figure shows the two transistors connected in the form of transmission function logic. In this circuit b is the control input .The gates of pmos and nmos are connected to each other. b is connected to the gates of pmos and nmos. a is input to pmos and a' is input to nmos .When b=0 ; pmos is on , nmos is off , thus the output will be a. when b=1; pmos is off ,nmos is on ,thus the output will be a'.

Table 1. Truth table of TFL

a	b	f
0	0	0
0	1	1
1	0	1
1	1	0

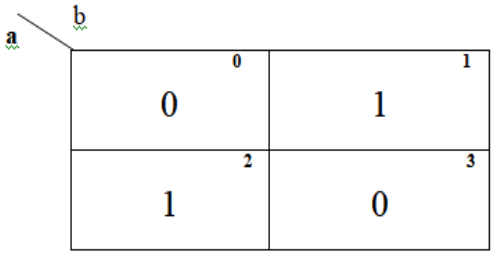

Figure 3: K Map of TFL

By solving k map we get F=ab'+ a'b

By observing the output expression we can note that, at the input only input b is given and in the output b' is automatically generated. Thus it can be concluded that by using the transmission function logic, the number of transistors used in building a circuit can be reduced.

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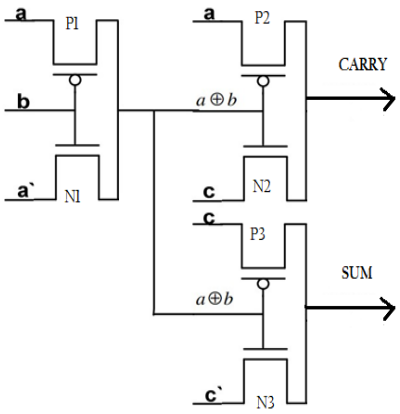

Figure 4: 6T Full Adder circuit

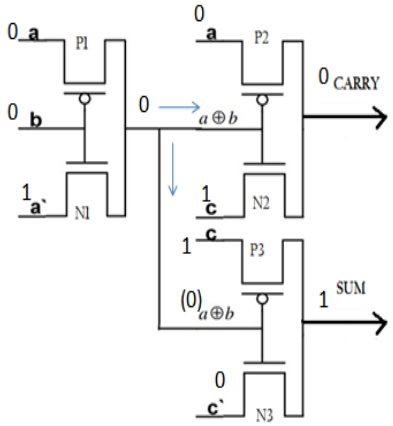

Figure 5: 6T Full Adder When control input b=0

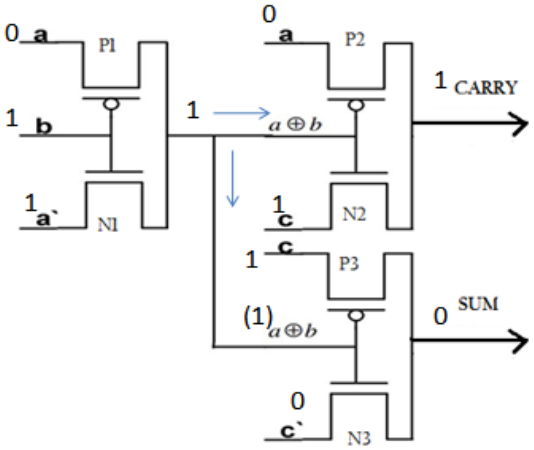

Figure 6: 6T Full Adder When control input b=1

Table 2. 6T Full Adder Input Specifications

Specifications	A	Abar	B	C	Cbar
Voltage 1(v)	0	1.8	0	0	1.8
Voltage 2(v)	1.8	0	1.8	1.8	0
Period (ns)	120	120	80	40	40
Raise time (ps)	500	500	500	500	500
Fall time(ps)	500	500	500	500	500
Pulse width(ns)	60	60	40	20	20

IV. RESULTS AND DISCUSSION

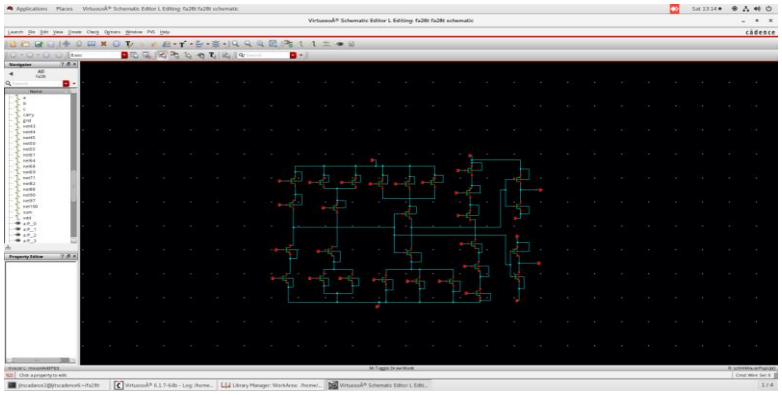

Figure 7: 28T Full Adder circuit schematic

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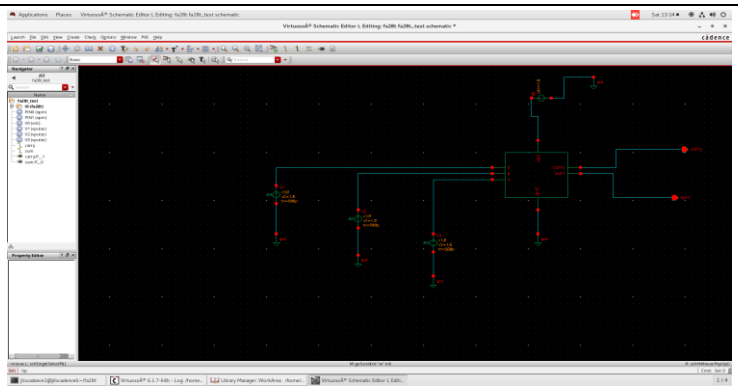

Figure 8: 28T Full Adder test schematic

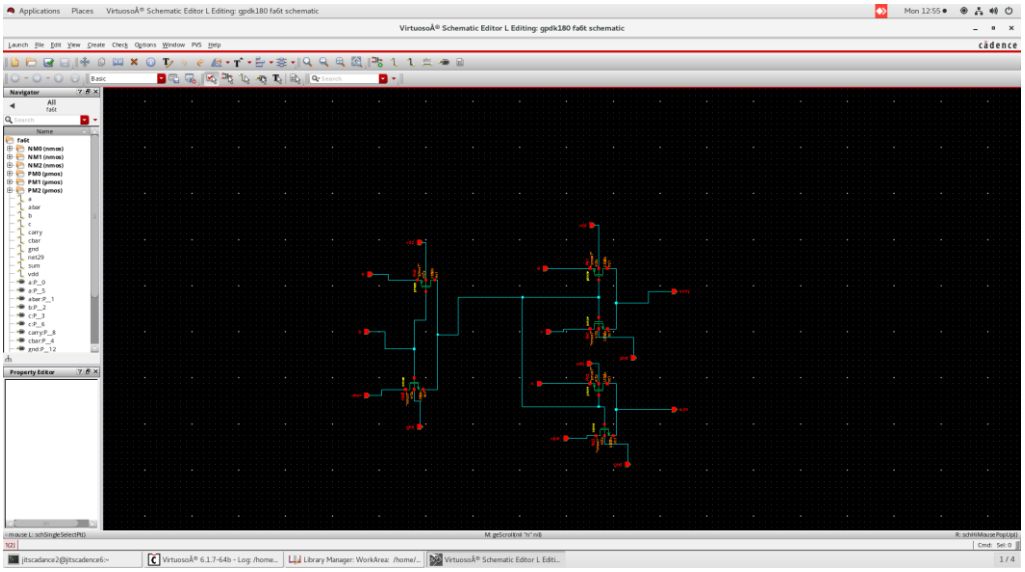

Figure 9: 6T Full Adder circuit schematic

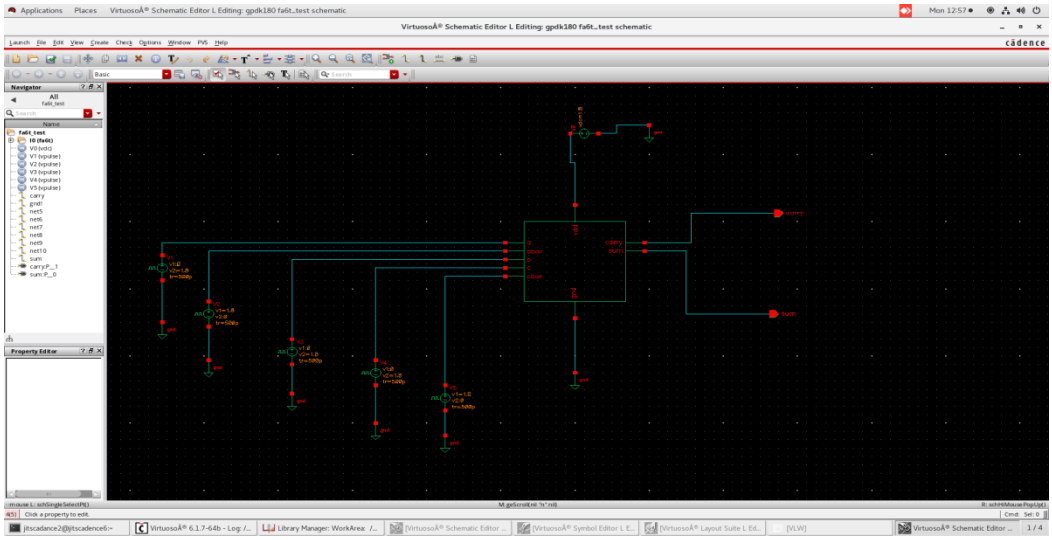

Figure 10: 6T Full Adder test schematic

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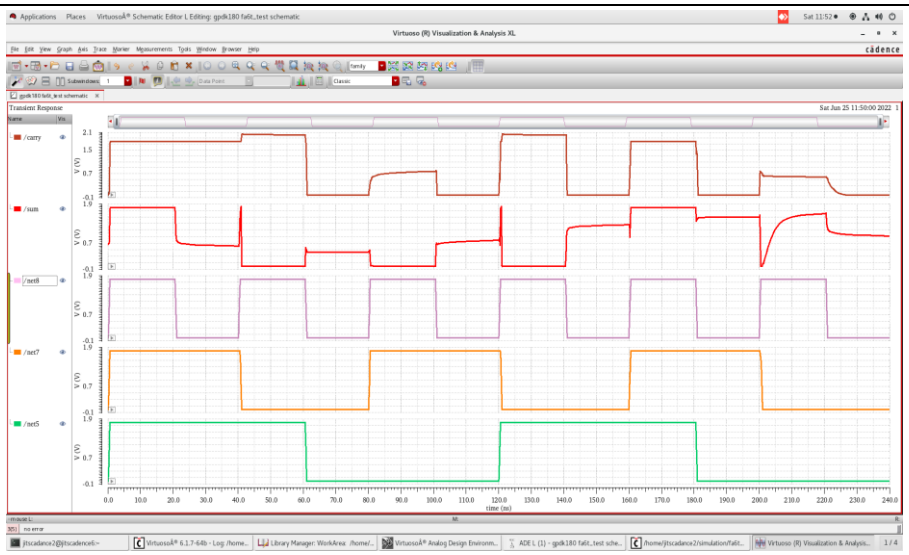

Figure 11: 6T Full Adder circuit output waveforms

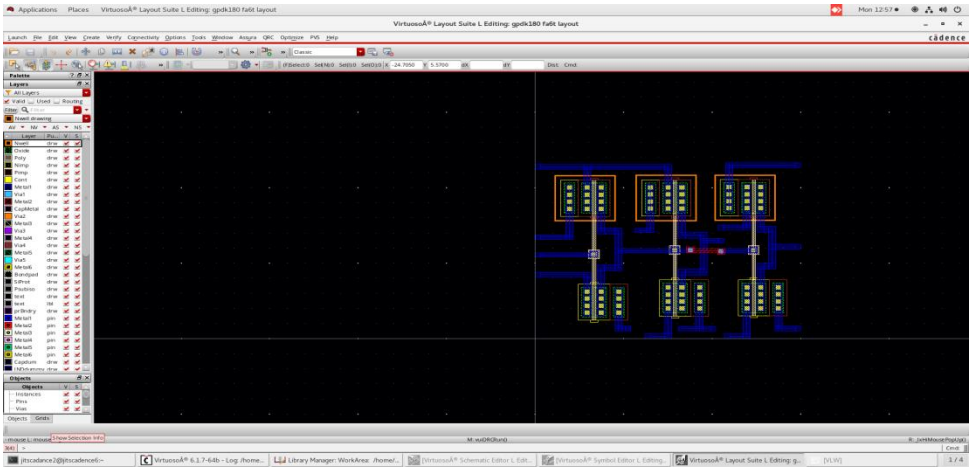

Figure 12: 6T Full Adder layout

Table 3. Logic flow in 6T Full Adder circuit

a	b	c	a'	c'	P1	N1	P2	N2	P3	N3	Sum	Carry
0	0	0	1	1	ON	OFF	ON	OFF	ON	OFF	0	0
0	0	1	1	0	ON	OFF	ON	OFF	ON	OFF	1	0
0	1	0	1	1	OFF	ON	OFF	ON	OFF	ON	1	0
0	1	1	1	0	OFF	ON	OFF	ON	OFF	ON	0	1
1	0	0	0	1	ON	OFF	OFF	ON	OFF	ON	1	0
1	0	1	0	0	ON	OFF	OFF	ON	OFF	ON	0	1
1	1	0	0	1	OFF	ON	ON	OFF	ON	OFF	0	1
1	1	1	0	0	OFF	ON	ON	OFF	ON	OFF	1	1

Table 4. 28T Vs 6T

Full adder designs	Conventional(28T)	Proposed (6T)
Count delay(nS)	0.371	0.363
Average Power Consumption(uW)	52.5	3.81
Number of Transistors	28	6
Power* Delay(uW.nS)	19.4775	1.38303

The area is reduced by 53% when compared to conventional 28 transistor full adder. Power, delay are calculated using the calculator available in cadence virtuoso tool.

V. CONCLUSION

A 6 transistor 1 bit full adder is implemented using Cadence virtuoso tool at 180nm technology by at a supply voltage of 1.8V. By implementing the circuit using transmission function logic there is a considerable change in parameters .According to the simulation results 92.74% less power consumption , the area is reduced by 53% and 92.89% less power delay product when compared to conventional 28t full adder.

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