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IMPLEMENTATION OF LOW POWER 17-TRANSISTOR TRUE SINGLE -PHASE CLOCKING FLIP –FLOP DESIGNS WITH 45 NM CMOS TECHNOLOGY

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ABSTRACT

Flip- Flops(FFs) are the fundamental storage components abundantly used in digital system designs which involves pipelining structure and modules built by FFs. The FFs contribute a major amount to total power consumption and significant amount to chip area of there digital system .so there is a need for low power and low area FF designs .in this paper low power 17 –True single-phase clock (TSPC) method of reasoning has found wide use in advanced plan. flip –flop in 45 nm CMOS is proposed .the logic structure of proposed TSPC FF of master –slave type in which master –stage is formed by static CMOS logic and slave informed by a mixed combination of static CMOS logic and complementary pass transistor logic .the proposed TSPC FF circuit is fully static because no internal nodes are in floating state during the operation which actually prevents leakage power dissipation .the proposed TSPC FF is designed by optimizing 17-transistor logic structure reduction flip –flop (LRFF) with respect to area and power consumption ,but without compromising the functionality of the FF. the design of three FFs namely transmission gate based flip –flop (TGFF),LRFF and proposed TSPC FF are implemented and simulated using gpdk 45 nm technology library with supply voltage vdd of 1v and clock frequency of 500mhz in DSCH and MICROWIND tool.

Keywords: TSPC, VLSI, Flip-Flop, RAM, ROM, SRAM.

I. INTRODUCTION

Two vital attributes of CMOS gadgets are high clamor invulnerability and low static power utilization .Since one transistor of the match is constantly off, the arrangement blend draws huge power just quickly amid turning among on and off states. Subsequently, CMOS gadgets don't create as much waste warmth as different types of rationale, for instance transistor-transistor rationale (TTL) or N-type metal-oxide-semiconductor rationale (NMOS) rationale, which ordinarily make them stand current notwithstanding when not evolving state. CMOS additionally permits a high thickness of rationale works on a chip .It was fundamentally therefore that CMOS turned into the most utilized innovation to be executed in very-large-scale integration (VLSI) chips.

"CMOS" alludes to both a specific style of advanced plan and the group of procedures and used to executes that hardware on coordinated circuits (chips). CMOS hardware disperses less power than rationale families with resistive burden . Since this preferred standpoint has expanded and developed more essential, CMOS procedure and variations have come to overwhelm, accordingly most by far of present day coordinated circuit fabricating is on CMOS forms [1].

CMOS circuits utilizes a blend of p-sort and n-type metal-oxide-semiconductor field-effect transistor (MOSFETs) to execute rationale doors and other advanced circuits. Despite the fact that CMOS rationale can be executed with discrete gadgets for showings, business CMOS items are incorporated circuits made out of up to billions of transistor of the two sorts, on a rectangular bit of silicon of somewhere in the range of 10 and 400 mm2.CMOS dependably utilizes all improvement mode MOSFETs[2].

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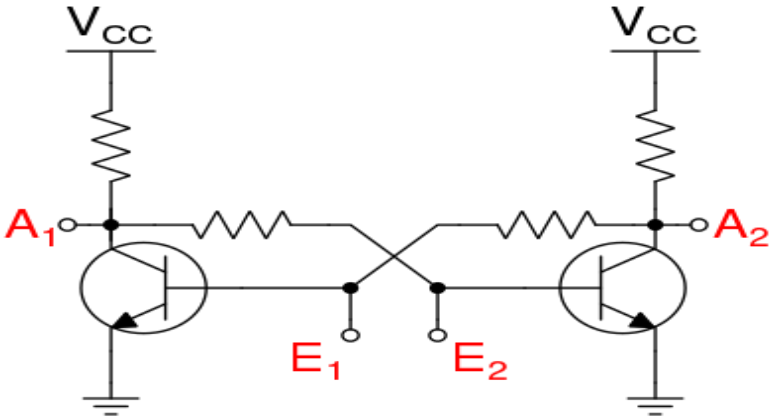

Figure 1: A traditional (simple) flip-flop circuit

Flip-flop are the fundamental storage elements in digital system design which are used to implement pipelining structure more than 50% of random logic power in a chip of soc is consumed by their inessential transition of internal nodes when the output and the input are in the similar state various low power techniques have been discussed ,but all of them bear transistor –count strafe ,salient to an increase in size which is too expensive .the conventional TGFF has two clock buffers inverters which coherent use power in every clock cycle further activity of low data activity to reshuffle these clock buffers we recognize a topology of differential master –slave .since the evolution of internet of things (IoT) and wearable devices are increasingly the requirement for ultra –low power circulation SOC chip is rising as well. The most optimum path to decrease power is to reduce the voltage so the scruting of circuit operation in near threshold & sub-threshold voltage have been introduced and dissertate widely .design of digital circuit mostly assign extensive flip-flop for buffering of data or pipelining ,and the circuit capacity of FF design expansively possesses the overall consumption of power and chip area. The proposed design 17- transistor is optimizing of 18-transistor TSPC FF.

This paper represents a new flip –flop definite to as true single –phase clocking flip-flop (TSPCFF) that fulfill the need above ;it is static fully contention –free and uses clocking of single –phase. the device count is almost same as a TGFF with layout size rises that equal to a single poly-pitch increase in 45nm technology. An external advantage of the TSPC topology is that it clarify the "hold –time way" collate to a regular TGFF.

True Single Phase Clock(TSPC) is a general unique flip-flop that works at fast and expends low power .The capacity of a clocked storage component is to catch the data at a specific minute in time and protect it as long as it is required by the advanced framework. computing of near threshold obligation dramatic improvements in every capacity . for many CMOS design s the consumption of energy reaches an minimum in the NTV(near threshold voltage) regime that is of the series of magnitude reformation over super threshold operation .however degradation of frequency due to voltage scaling may be permitted across all performance constrained or single –threshold applications enabling digital design to serve a over a large voltage range is way to obtain the bonzer energy efficiency while good varying application execution demands to tap the full latent feasible of NTC multilayered co-optimization reaches that cross cut devices ,architecture ,design ,circuit methodology and tool flows and connect with techniques of fine –grain power management are compulsory to realize NTC circuit and scaled CMOS process nodes .

TRUE SINGLE PHASE CLOCK ARCHITECTURE

Most integrated circuits (ICs) of satisfactory unconventionally use a clock signal with the true objective to synchronize various pieces of the circuit cycling at a rate slower than the most negative situation inside delays . on occasion, more than one clock cycle is required to play out a for seen movement .as ICs end up being more incredible the issue of giving careful and synchronized clocks to all of the circuits ends up being continuously irksome .the extraordinary instance of such complex chips is the microchip ,the central piece of present day PCs ,which relies upon a clock from a valuable stone oscillator .the principle uncommon cases are non simultaneous circuits ,for instance ,offbeat CPUs .

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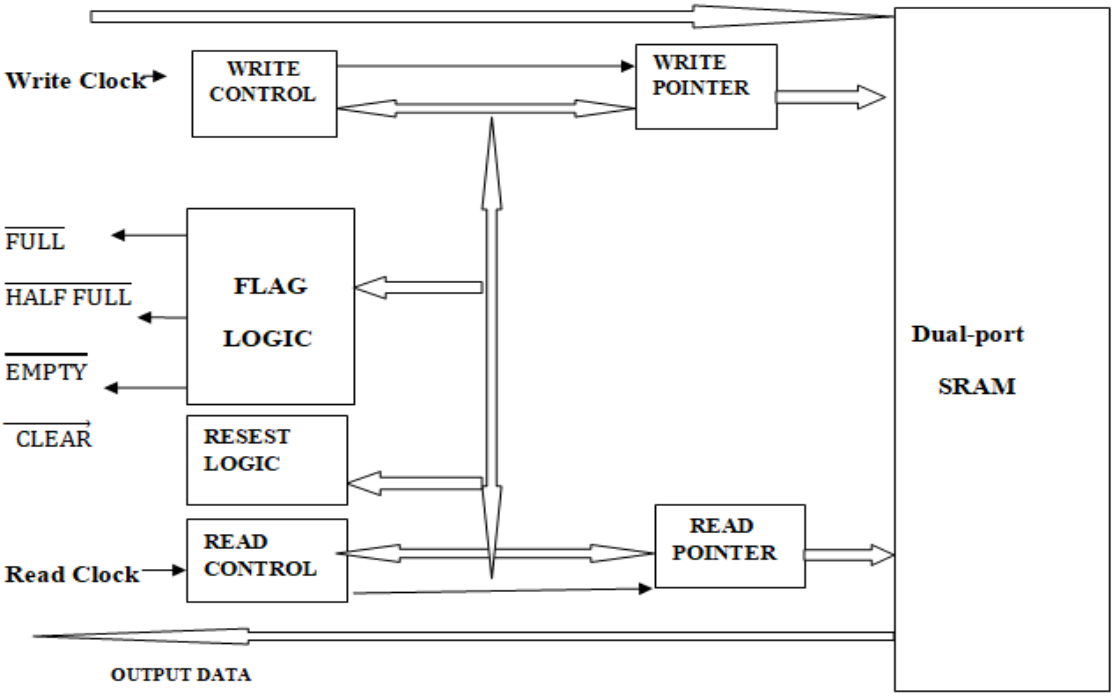

Figure 2: Block diagram of FIFO with storage

In figure 2 a long fall-through time in long FIFO the designing ought to never again more the data words through all memory territories .the issue is comprehended by an indirect FIFO thought ,the memory address of the moving toward data is in the create pointer .the area of the primary data is in the create pointer .the area of the primary data word in the FIFO that will be examined out is in the scrutinized pointer .after reset ,the two pointers show a comparable memory region .after each make task the make pointer is set to the following memory territory

Step 1- Firstly make design in DSCH software using available component then make connection between them as per requirement .

Step 2-Now press run simulation and see output in terms of LED glow or not ,if input and clock is on and glow then designed circuit give proper output otherwise there are some error in circuit.

Step 3-Now save this design and make Verilog file, then a Verilog file will be generated automatic.

Step 4-Open Microwind software and compile verilog file. then generate CMOS layout .now calculate parameters and compare result

This design proposes 17-transistor SPC (17TSPC) ,a SPC FF with only 17-transistors(the lowest reported for a fully static contention –free SPC FF) with novel master –slave fig.3.simulation results shows TCFF internal node voltage at (a) VDD=1.2v and (b) VDD=0.6v when D rising at CK=0, topology with a simplified topology ,it delivers a 20% reduction in cell area compared in 45-nm CMOS along with a TGFF .This proves EDA compatibility and demonstrates circuits and system-level benefits. The design was first simulated then experimentally validated at 0.7v 25 ^{0}c,at various data activity rate (a) showing that the proposed 17TSPC achieves reductions of 68% and 73% in overall(P_a=10%) and clock dynamic power(P_a=10%) ,respectively ,and 27% lower leakage compared to TGFF .furthermore ,unlike TCFF the measurement indicate superior 17 TSPC in performance.

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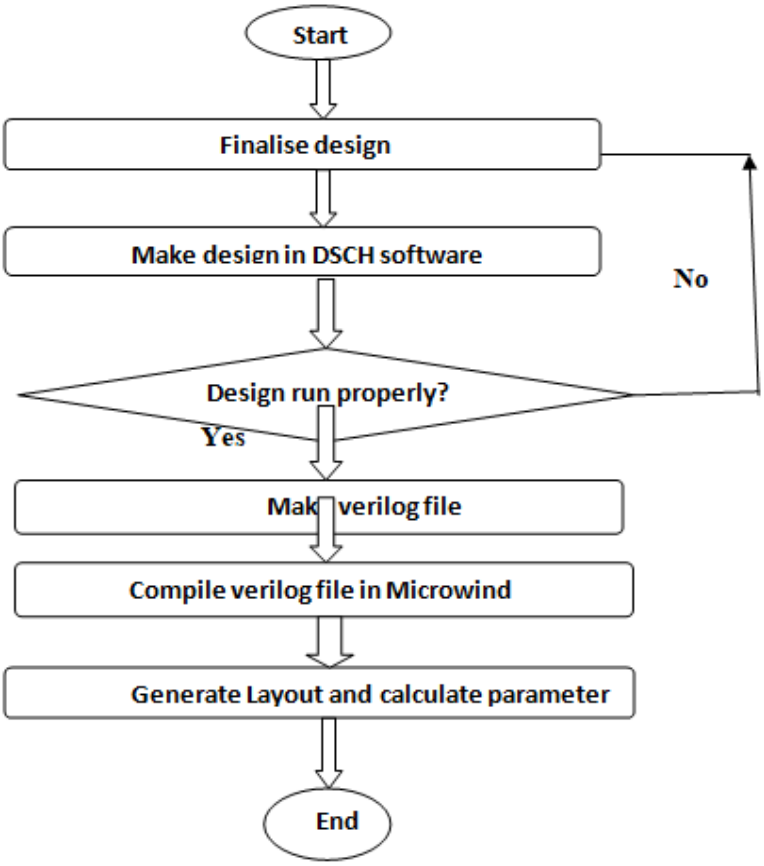

Figure 3: Flow Chart

The proposed design is compared with the other two static FF designs .the TGFF and the S2CFF.note that a TSPC based FF design using 17 –transistors is proposed in .

SIMULATION AND RESULT

The simulation studies involve the deterministic TSPC circuit as shown in fig.4 the proposed TSPC implemented with DSCH-Microwind software.

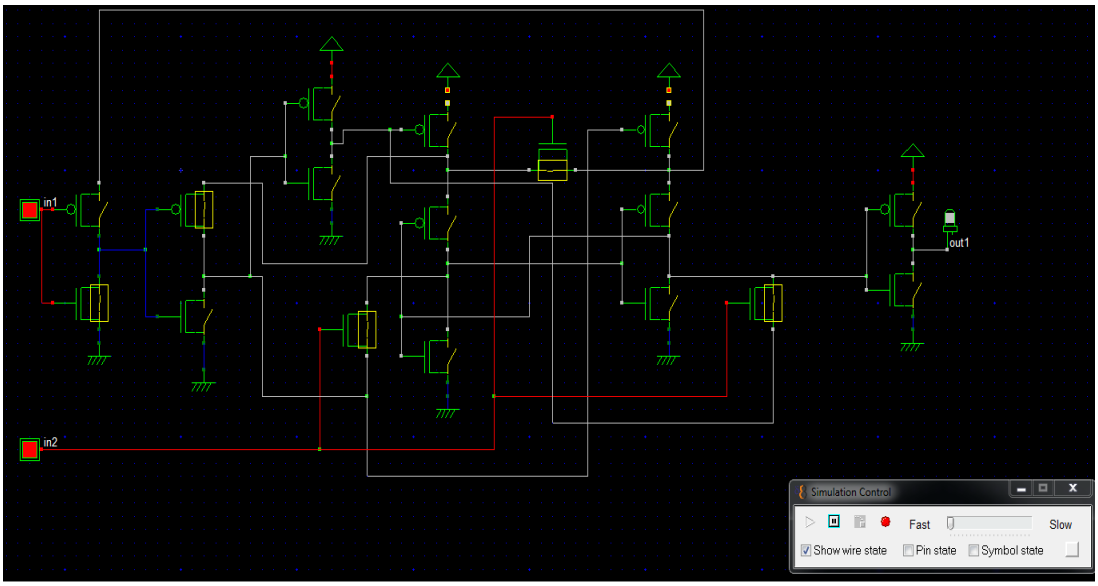

Figure 4: working of true single –phase clock flip-flop

however figure 4 showing design of transistor single phase clocked AND gate PMOS and NMOS components are using design this circuit to clock result when clk=1 d=1 then output =1

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Table 1: Truth table of TSPC FF

Clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

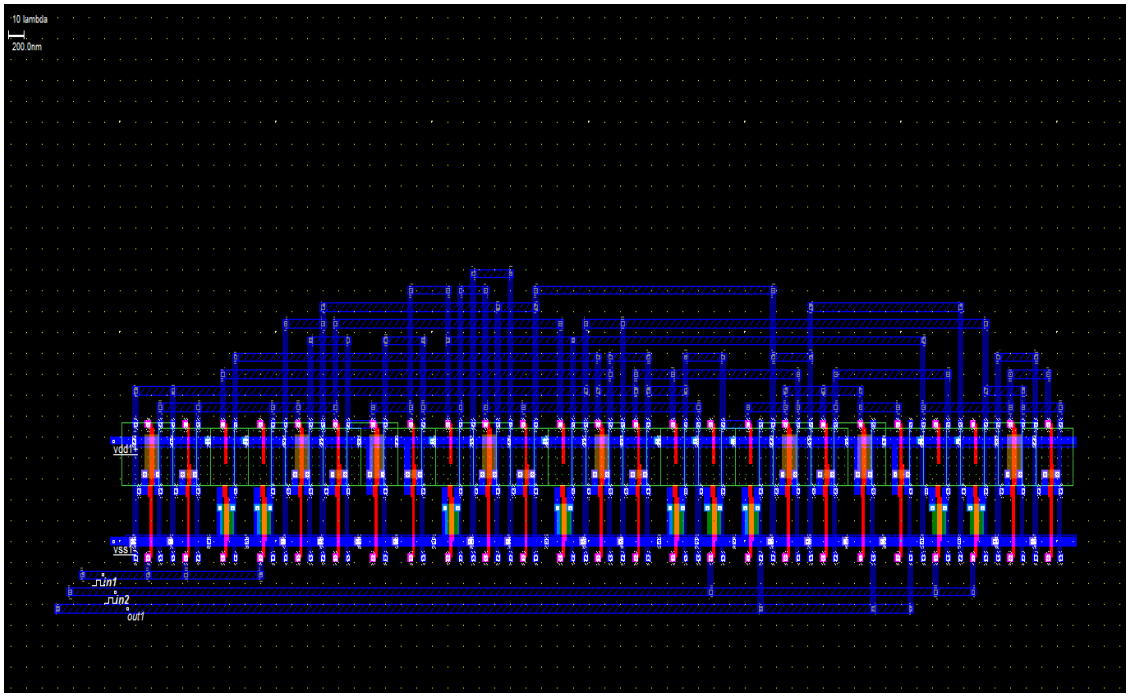

Figure 5: Proposed TSPC design circuit layout

Figure 5 presentation CMOS layout design of TGFF it includes various metal, PMOS, NMOS and contact points.

Table 2: Simulation parameter of proposed TSPC

Sr.No	Parameters	Value
1	Area	374.0µm2
2	Power	3.38µw
3	Delay	5ns
4	Power Delay Product(PDP)	625.28
5	Rise time	0.025ns
6	Fall time	0.025ns

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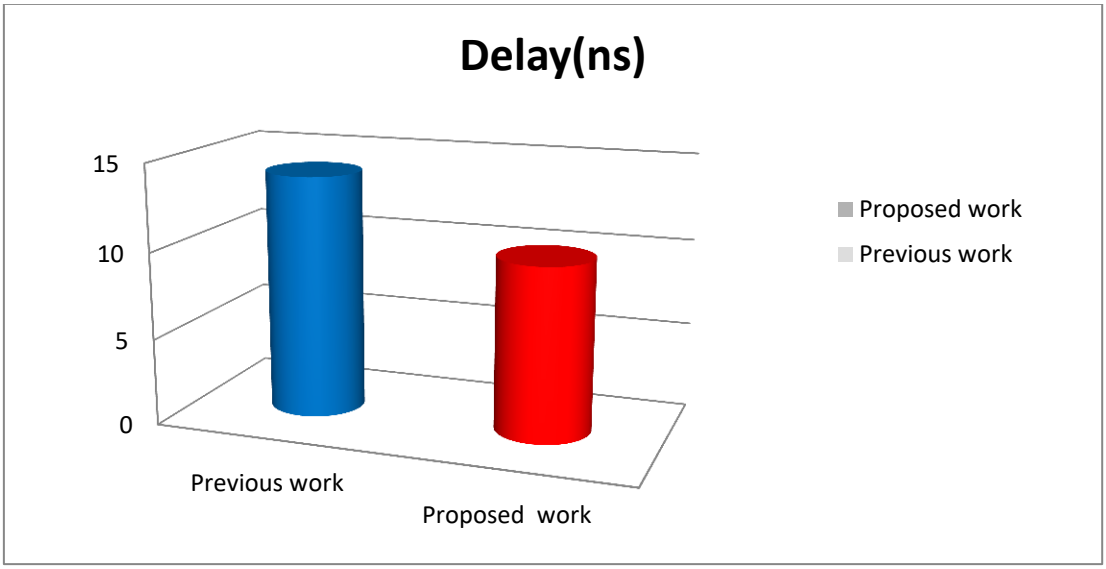

Figure 6: Delay plot of previous vs proposed design

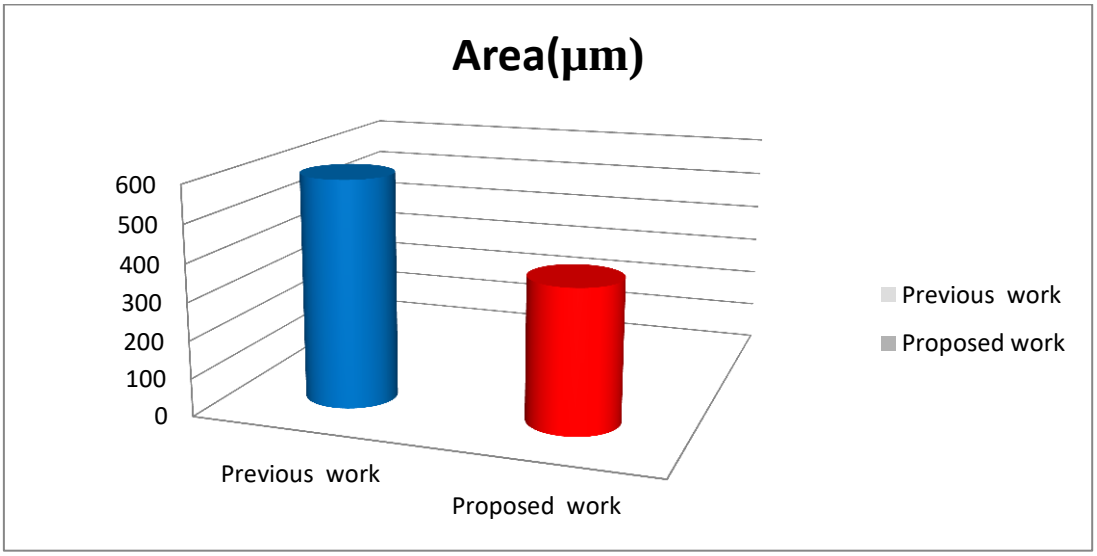

Figure 7: Area plot of previous vs proposed design

Therefore to see all simulated result and parameter values ,it is observed that proposed design performance is better than previous design. Improvement in parameters reduce transmission time and latency .the implementation and simulation of the proposed design is done over DSCH –MICROWIND software .the DSCH software has various menu and help bar ,where different gates supply ground etc are available , Microwind software also has the function which converts DSCH design into Verilog files and layout diagram .

II. CONCLUSION

This paper present a new flip –flop referred to as static single –phase contention –free flip-flop SPC FF with lowest reported number of transistors(17) ,demonstrating cell area reduction with respect to the conventional TGFF. Although penalty is observed ,thanks to low-power and uses single –phase clocking TGFF with layout size increase that corresponds to a one poly-pitch increase in 45nm technology .in order to achieve reliable energy –efficient operation across a wide operating voltage range a ,single –phase clocking which avoids toggling of internal clock inverters and the corresponding power penalty .A brief summary of the proposed 17TSPC and comparison with prior works is presented .therefore the proposed 17TSPC has better power characteristics than the previous.

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