e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:04/Issue:02/February-2022 Impact Factor- 6.752 www.irjmets.com

DESIGN AND IMPLEMENTATION OF SS- ADC COMPONENT USING FINFET TECHNOLOGY

Mahadevi S.Manur*1, Dr. Kiran Bailey*2

*1Assistant Professor & Research Scholar, Dept Of ECE, Don Bosco Institute Of Technology, Bangalore, 560074, Karnataka, India.

*2Assistant Professor, Dept Of ECE, B.M.S College Of Engineering, Bangalore, 560019, Karnataka, India.

ABSTRACT

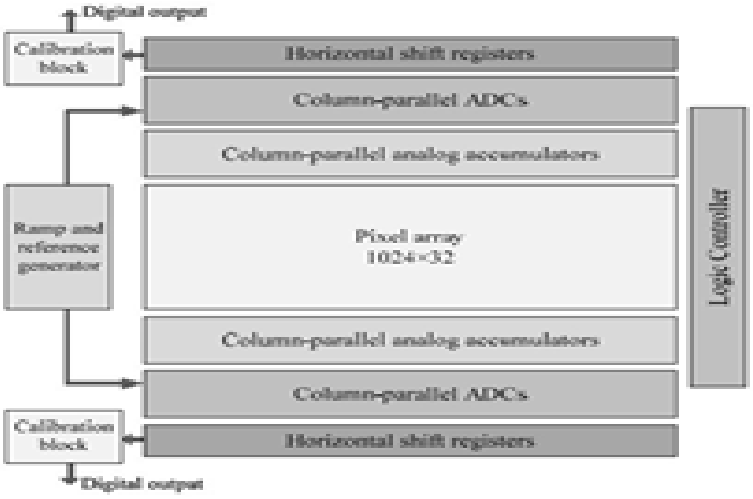
CMOS Image Sensors are integrated by the analog to digital converter technology as a system on chip (SoC) portable devices. Analog-to-digital converter (ADC) become the primary requirement because power consumption of column parallel ADC in CMOS image sensors plays significant role in total power regulation. The column parallel ADC is one of the important technology which helps in achieving high pixel rate from CMOS image sensors. Single gate MOSFETs are sufficient for deigning of the sub micro region. Single gate MOSFETSs cause short channel effects which impacts performance criteria when the designing moves down to ultra sub region. The ultra sub region can be effectively designed using Multi gate MOSFETs. By moving to FinFET technology, the benefits gained in power savings are more pronounced than the performance improvement achieved. Hence SS-ADC architecture is selected to implement in 14nm FinFET Technology.

Keywords: ADC, CMOS Image Sensors, Finfet Technology, Mosfets, Short Channel Effects.

I. INTRODUCTION

To ensure the digital processing on the digitized signal the method of conversion must be implemented. ADCs are one of the basic building blocks which takes care of analog signal processing, storage, and transformation into digital form. An embedded integrated chip functioning involves conversion of analog to digital converter. The continuous developments of ADCs are the results of the growing demand of higher data rates and lower cost. The conversion of the analog signals which are continuous amplitude into discrete time and discrete amplitude signal. There are many functions carried out by ADC which includes sampling, quantizing, encoding and transformation of continuous quantities to discrete quantities. The outcome of ADC comprise of errors because of the finite resolution of ADC and electronic components variations.

CMOS Image Sensors are integrated by the analog to digital converter technology as a system on chip (SoC) portable devices. Analog-to-digital converter (ADC) become the primary requirement because power consumption of column parallel ADC in CMOS image sensors plays significant role in total power regulation. High pixel rate can be achieved from CMOS image sensors only integrated with the column-parallel analog-to-digital converter (ADC) technology.



e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:04/Issue:02/February-2022 Impact Factor- 6.752 www.irjmets.com

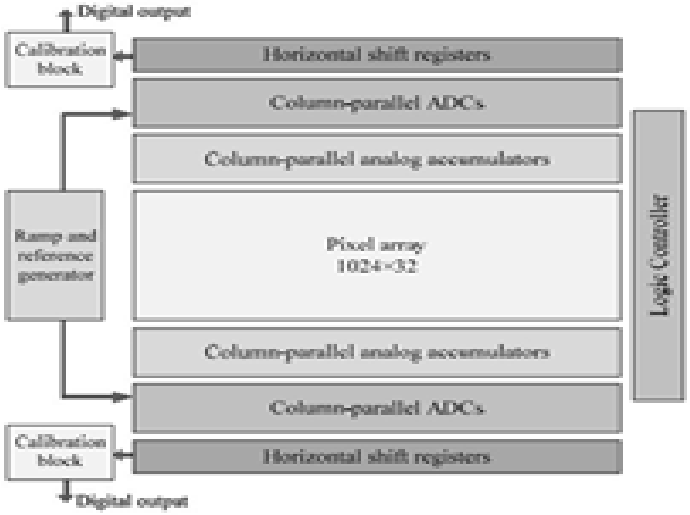


Figure 1: Block Diagram of Image Sensor

The outputs from ADC technology where analog to digital conversion of pixels shows the image quality, image layouts and frame rate.

Wide dynamic range image sensors that has a feature of high speed processing are required for industrial and machine vision imaging applications [1]. The feature of on chip parallel image processing with very low power consumption can be achieved only with the use of CMOS image sensors for these applications. Figure 2 shows the basic architecture of on sensor parallel image processing system. Analog to digital converter (ADC) arrays are used for digitizing he column parallel image data. Column parallel processing array helps in processing the digitized data. The architecture is apt for the image processing with certain criteria's such as maintaining high fill factor and high sensitivity of image array [2]. Performance of the column ADC limits the speed and range of the proposed architectural model.

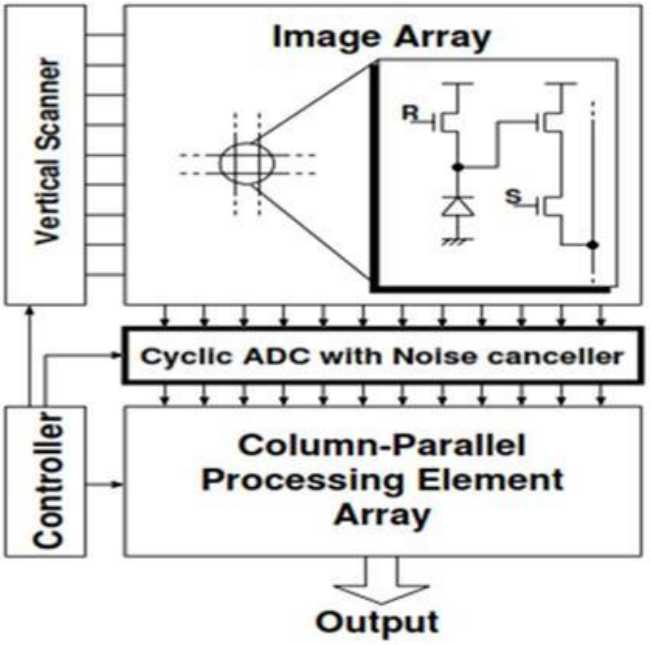


Figure 2: Basic architecture of image processing system

II. EVOLUTION OF FINFET

Scaling, controlling the design metrics and power optimization forms the most important factors for any technology. Single gate MOSFETs are sufficient for deigning of the sub micro region. Single gate MOSFETSs cause short channel effects which impacts performance criteria when the designing moves down to ultra sub region. The ultra sub region can be effectively designed using Multi gate MOSFETs called FinFETs

e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:04/Issue:02/February-2022 Impact Factor- 6.752 www.irjmets.com

Achiveing distinctive device parameters becomes challenging due to the continued shrinkage of the process technologies beyond 22 nanometers (nm). Scaling of dynamic power especially in the power supply voltage is difficult using the CMOS transistor scaling. In order to achive the required scaling in the power supply voltage FinFET based multi gate are used for replacing the existing technologies.

FinFET is the multigate MOSFET (metal-oxide-semiconductor field-effect transistor). The structure of FinFET is built on the substrate where two, three or four sides of the channels are placed with gates that foms the multi gate structures. Since source of FinFETs forms the fins on silicon surface these devices are given a name of "FinFETs". When compared to CMOS (complementary metal-oxide-semiconductor) technology, FinFET devices have higher density and have

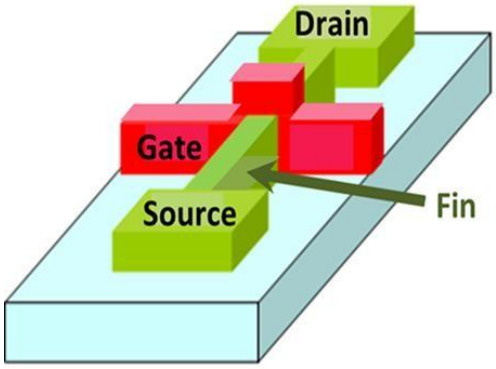


Figure 3: Fin field-effect transistor (FinFET)

FinFET is classified as the type under 3D transistor and therefore forms the basis for the fabrications of nanoelectric semiconductors. FinFETs were aggressively utilized in microchips during early 2010s and they became dominant with their implementation when the gate designs were developed at 7 nm, 10 nm, and 14 nm process nodes. In order to drive the performance and strength of electronic systems, FinFET transistor can be arranged side by side with multiple fins which are covered using same gates [18].

2.1 Overcome of short-channel-effects in FinFET

There will be an imposition of the drain current from source and drain regions due to the parasitic electric fields. MOSFETS are capable of controlling drain current as they hold supreme control over the channel. Because of the channel length being in order with the source and drain regions, the short channel devices do not get enough control of the channel resulting in short channel effects. Whereas in FinFETs these gates are present all over the channels provides enhanced control over the channels. The figure 4 shows how electric fields travels from source and drain. The representation shows that the electric fields from source and drain regions are ended in second gate which makes the channels completely free, providing authority over the channel which is desired.

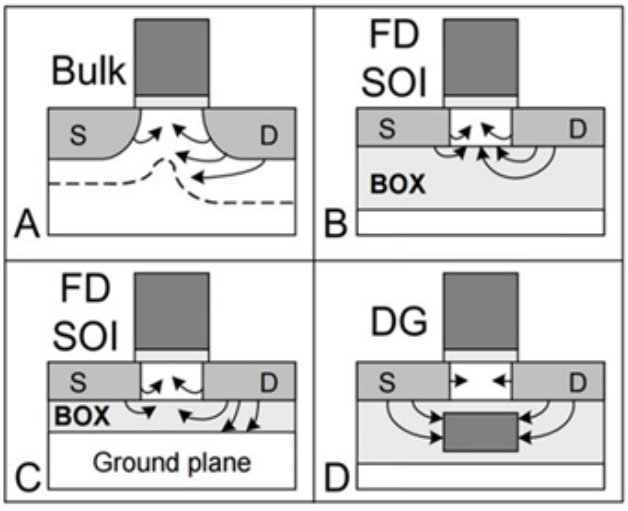


Figure 4: short-channel-effects in FinFET

e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:04/Issue:02/February-2022 Impact Factor- 6.752 www.irjmets.com

III. SYSTEM ARCHITECTURE AND ARCHITECTURE OF CMOS SENSOR

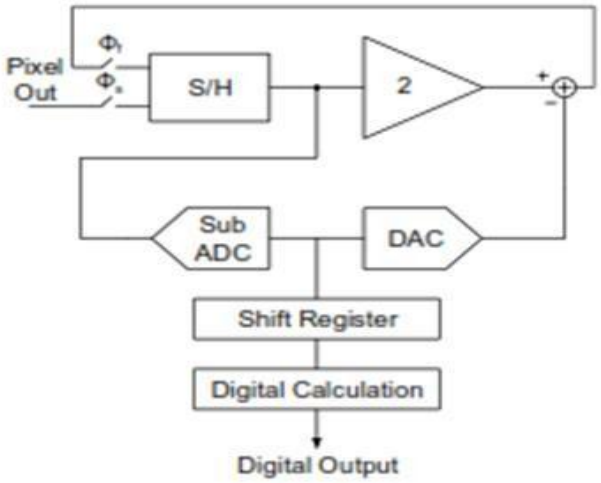


Figure 5: System architecture

Cyclic ADC system architecture is shown in figure 5 [18]. The pixel output signal is sampled by closing sampling switch ΦS. Until the next sampling period comping the sampling switch ΦS should be kept open. The second part of the system architecture shows that the sampled signal should pass through two parts. First part is sub ADC and another part is multiplier. Sub ADC provides 1.5 bit of digital codes. The part of the system functioning involves in transformation of digital codes to analog signals by DAC. The output of analog signals are then subtracted by the input signals to generate the residue signal which is gained 2.

The two steps are the fundamental steps to all the 11 conversion cycles . The input signal and sampling switched are replaced to residue signal obtained from last time and Φf. The 1.5 bit digital codes acquired during each conversion step are transferred to shift register and stored. The digital calculation blocks are used to compute final digital bits from groups of digital codes after 12 sampling clock periods [3]

The block diagram of the ADC in the architecture for ultra high definition TV which uses CMOS image sensor is as shown below

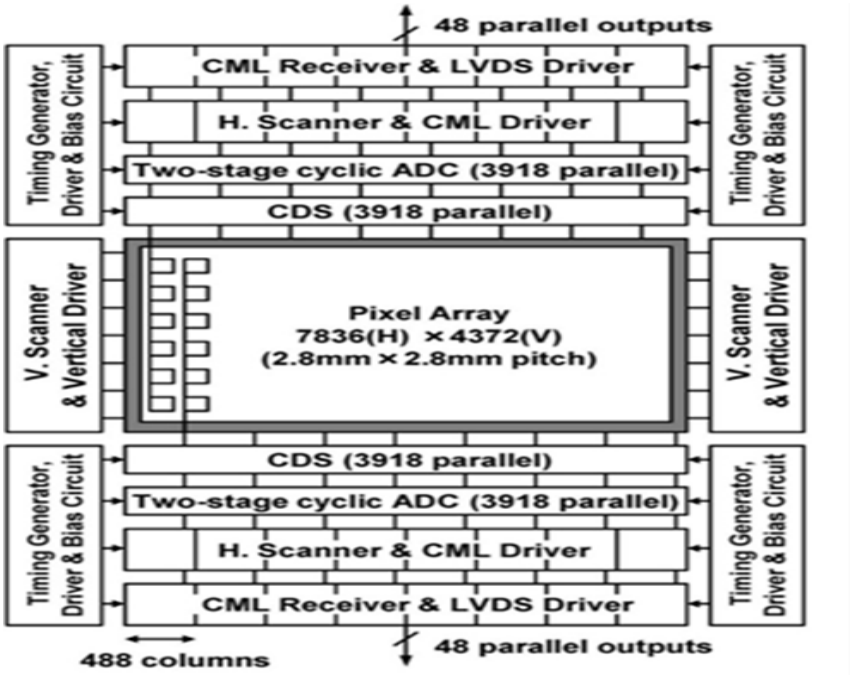


Figure 6: Architecture of CMOS image sensor.

Architecture of the SHV image sensor for ultra-high-definition TV. CML: Current mode logic. LVDS: Low-voltage differential signaling (digital data transfer circuit). CDS: Correlated double sampling (noise reduction circuit). ADC: Analog-to-digital converter.

e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:04/Issue:02/February-2022 Impact Factor- 6.752 www.irjmets.com

IV. DESIGN AND IMPLEMENTATION

The required image specifications for SHV video signals are 4320 lines of 7680 pixels, with 12 bit resolution and 120 frames/s (fps). Readout capability is essential to match this specification and transfer of high-speed data. The SHV sensors read the total pixel output at 47 Gb/s or more. To achieve a high pixel rate from a CMOS image sensor, ADC is essential technology. Many digital cinema applications utilize the ADC architecture via the image sensors [3]-[6]. Even with these specifications and applications do not meets the required specifications for SHV. The image sensor that matches the half of the specifications required for the full SHV specifications is 33-megapixel, 60 fps CMOS image sensor which has the tool of successive approximation column parallel ADC [5]. The 33- megapixel CMOS image sensors is recorded with the consumption of power value of 3.7 W. Another image sensors which show similar features of matching half the resolution required by SHV specifications is 17.7-megapixel 120 fps CMOS image sensors that comprise of single slope column parallel ADC [6]. The 17.7-megapixel 120 fps CMOS image sensors uses very high clock frequency that helps in achieving high speed analog to digital transformation. The column parallel ADCs are used in many forms in several image sensors: cyclic ADC [7], [8], and delta sigma ADC [9].

A/D transformation time is less in cyclic ADC which makes them apt for use in high speed image sensors. One disadvantage of cyclic ADCs is that they contain amplifiers that results in more power consumption when compared to other ADCs. Whereas high bit resolution and low temporal noise can be expected from Delta ADC because they rely on the oversampling technique. The number of samples required for generating 12 bits is 90 which is more when compared to other cyclic ADCs. [14] describes much in detail about the use of column-parallel two-stage cyclic 12-bit ADCs.

Table 1. Comparison with recent high-resolution image sensors

Ref.	[4]	[6]	[9]	[8]	[13]	This work
Resolution [bits]	12	12	12.5	13	12	12
Technique used	SAR	SS	ΔΣ	Cyclic	2-Stage cyclic	2-Stage cyclic
Frame rate [fps]	60	120	120	360	1700	120
# of V. pixels	2168	2160	1212	428	1024	4320
# of H. pixels	4122	8192	1696	640	1280	7680
Noise [e-]	2.8	2.75	2.4	4.5	7	3.0
Colum Amp. gain	8	11.2	1	1	2	7.5
Conv. gain [μV/e-]	45	48	80	61	40	63
Power [mW]	1085	3000	180	297	908	2670
FoM [e-·nJ]	5.7	3.9	1.8	13.6	2.9	2.0

By moving to a 14 nm FinFET technology, the advantages gained in power savings is more pronounced than the performance improvement achieved. From the above table, the SS-ADC architecture implemented in [6] consumes the maximum power and stands to gain most by implementing FinFET technology. Therefore an SS-ADC architecture is selected to be implemented in 14nm FinFET Technology.

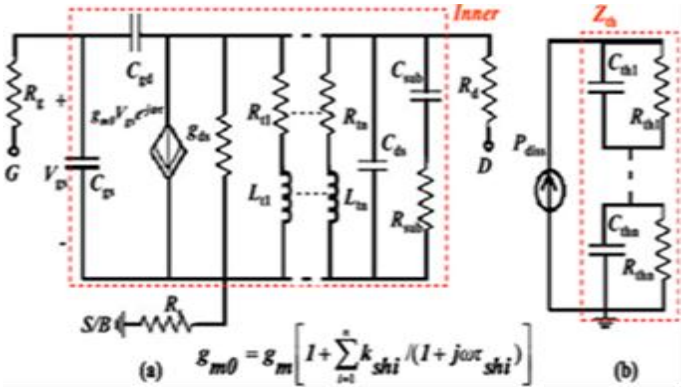


Figure 7: FinFET Equivalent Circuit model

e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:04/Issue:02/February-2022 Impact Factor- 6.752 www.irjmets.com

Small-signal Model Topology Development:

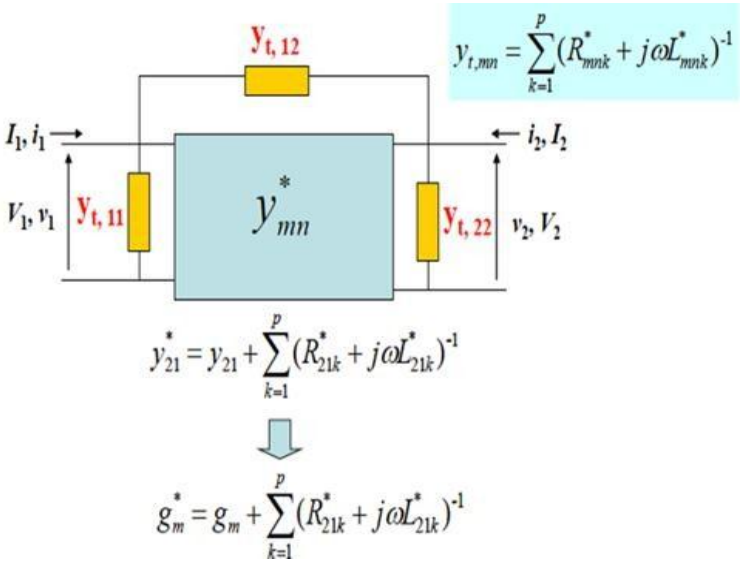


Figure 8: Small-signal Model Topology Development

Figure 8 shows the consideration of thermal feedback network and small signal equivalent circuit. The FinFET's intrinsic Y-parameters at low frequency can be written as:

$$Y^*_{21,\text{int}} = \left(g_m e^{-j\omega} - j\omega C_{gd}\right)\left(1 + \sum_{i=1}^{p} \frac{k_{thi}}{1 + j\omega\tau_{thi}}\right)$$

$$Y^*_{22,\text{int}} = g_{ds} + j\omega C_{ds} + \left(R_{sub} + \frac{1}{j\omega C_{sub}}\right)^{-1} + \sum_{i=1}^{p} \frac{1}{R_{ti} + j\omega L_{ti}}$$

$$Y^*_{11,\text{int}} = j\omega\left(C_{gs} + C_{gd}\right)$$

$$Y^*_{12,\text{int}} = -j\omega C_{gd}$$

4.1 Comparator Stage – Implemented using CMOS

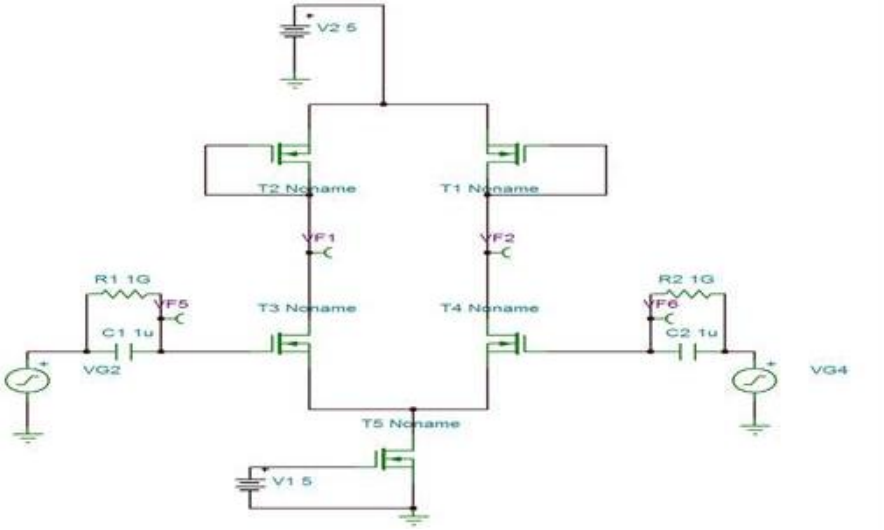


Figure 9: Comparator Stage – Implemented using CMOS

4.2 Comparator Stage – Implemented using FinFET

e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:04/Issue:02/February-2022 Impact Factor- 6.752 www.irjmets.com

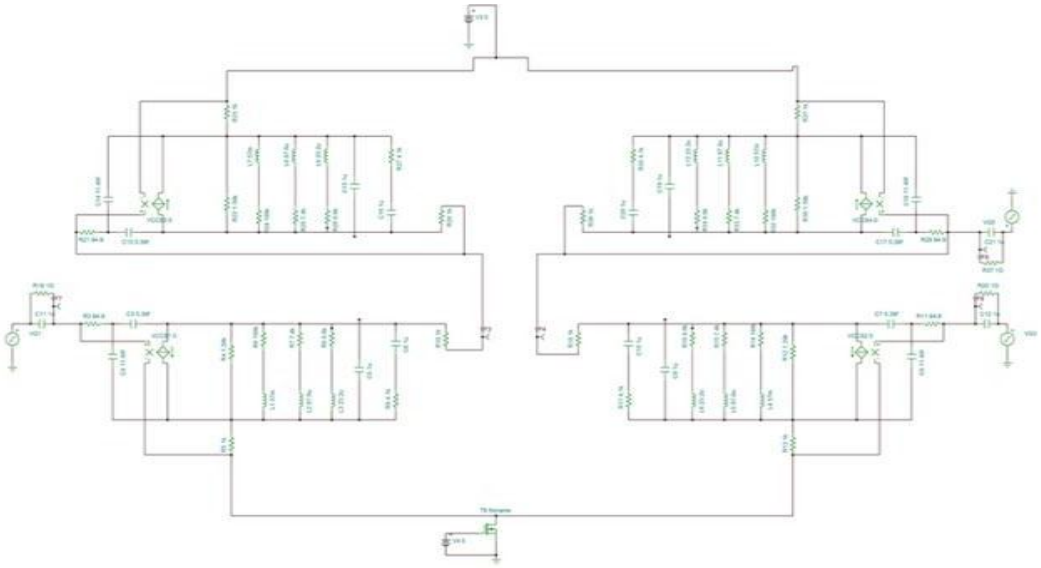


Figure 10: Comparator Stage – Implemented using FinFET

V. RESULTS AND DISCUSSION

ADC Target Specification

The required bit depth is 12 bits which means a clock of at least 2.76 GHz is required to be used. The pre-amp and regenerative switch is used due to its low power characteristic[15]. Different FinFET models exist based on different parameter extraction methods and each model has its own set of abstraction or approximation. Therefore the limitation of each FinFET model needs to be understood before using the model and this paper uses the FinFET model [16]. The pre-amp circuit in [15] being the power consuming is implemented using the FinFET model in [16].

CMOS Out and Fin Out waveforms

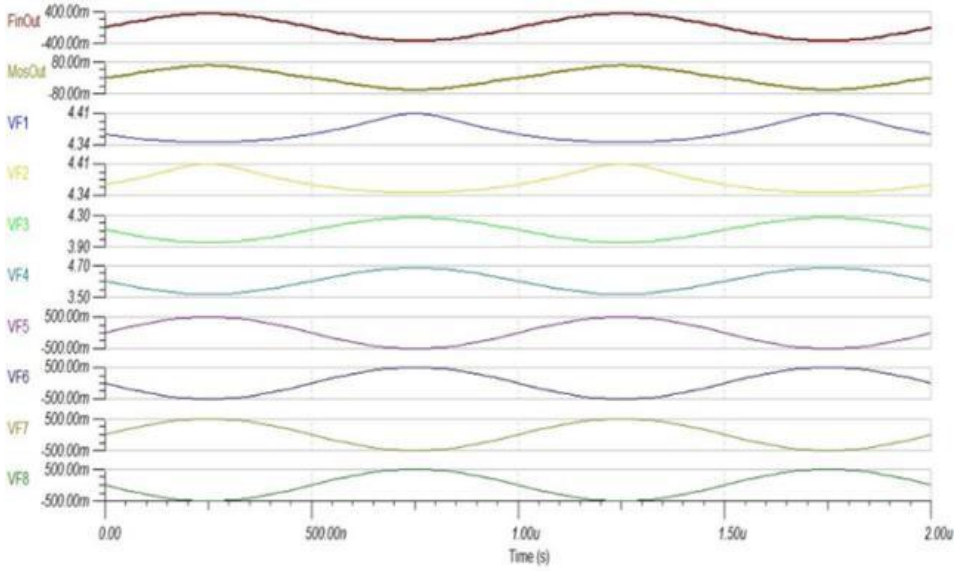


Figure 11: Input and Output of the comparator stage for both the models

VF5 and VF6 are the differential inputs and VF1 and VF2 are the differential outputs of the CMOS comparator. VF7 and VF8 are the differential inputs and VF3 and VF4 are the differential outputs of the FinFET comparator.

VF5 and VF7 are identical. VF6 and BF8 are identical. Both the comparators are fed with the same input excitation. In real world, these excitations come from the CCD or pixels of the image sensor. The MOS Out and Fin Out waveforms are the outputs of the respective comparators.

e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:04/Issue:02/February-2022 Impact Factor- 6.752 www.irjmets.com

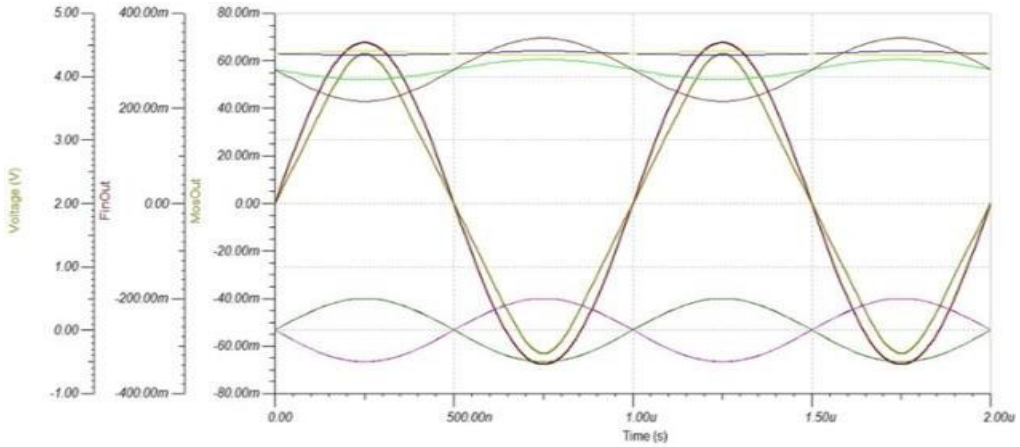


Figure 12: Input and Output of the comparator stage for both the models

It has been observed that the rise time of the FinFET model is fast than the CMOS model.

VI. CONCLUSION

A low-power ADC is the primary requirement due to the power consumption of column-parallel ADCs in CMOS image sensors play a vital role in total power consumption. To achieve a high pixel rate from a CMOS image sensor, the column-parallel analog-to- digital converter (ADC) is precise technology. The purpose has served with scaling up to sub-micro region by Single-gate MOSFETs but as designing moves down in ultra sub-micro region, additional scaling of single gate MOSFETs results a number of Short Channel Effects that directly impose the various performance criteria and to mitigate these effects, Multi-gate MOSFETs are existed . By moving to a 14 nm FinFET technology, the advantages gained in power savings is more pronounced than the performance improvement achieved.

From the above, the SS-ADC architecture implemented consumes the maximum power and stands to gain most by implementing FinFET technology. Therefore an SS-ADC architecture was selected to implement in 14nm FinFET Technology. Different FinFET models exist based on different parameter extraction methods. Each model has its own set of abstraction or approximation. The comparator circuits for SS-ADC have been implemented using CMOS and Fin FET models and Input and Output waveforms of the comparator stage for both the models have been obtained. It has been observed that the rise time of the FinFET model is fast than the CMOS model.

ACKNOWLEDGEMENT

The authors would like to thank Don Bosco Institute of Technology and B.M.S college of Engineering for all the tools support and encouragement provided by them to take up this research work and publish this paper.

VII. REFERENCES

[1] M. Sugawara, M. Kanazawa, K. Mitani, H. Shimamoto, T. Yamashita, and F. Okano, “Ultrahigh-definition video system with 4000 scanning lines,” SMPTE Motion Imag. J., vol. 112, no. 10/11, pp. 339–346, Oct./Nov. 2003 https://doi.org/10.5594/J16304

[2] T. Yamashita, K. Masaoka, K. Ohmura, M. Emoto, Y. Nishida, and M. Sugawara, “Super Hi-Vision video parameters for next- generation television,” presented at the SMPTE—Annu. Technical Conf. Exhibition, Hollywood, CA, Oct. 25–27, 2011 https://doi.org/10.5594/j18176

[3] I. Takayanagi, M. Shirakawa, K. Mitani, M. Sugawara, S. Iversen, J. Moholt, J. Nakamura, and E. R. Fossum, “A 1-1/4 inch 8.3 M-pixel digital output CMOS APS for UDTV application” in Proc. ISSCC Dig. Tech. Papers, Feb. 2003, pp. 216–217. https://doi.org/10.1109/ISSCC.2003.1234273

[4] S. Matsuo, T. Bales, M. Shoda, S. Osawa, B. Almond, Y. Mo, J. Gleason, T. Chow, and I. Takayanagi, “A very low column FPN and row temporal noise 8.9M-pixel, 60 fps CMOS image sensor with 14 bit column parallel SA-ADC” in Proc. IEEE Symp. VLSI Circuits, Dig. Tech. Papers, 2008, pp. 138–139. https://doi.org/10.1109/VLSIC.2008.4585983

[5] S. Huang, T. Yamashita, Y. Wang, K. L. Ong, K. Mitani, R. Funatsu, H. Shimamoto, L. P. Ang, L. Truong, and

B. Mansoorian, "A 2.5 inch, 33 Mpixel, 60 fps CMOS image sensor for UHDTV application" in Proc. Int. Image Sens. Workshop, Jun. 2009, pp. 308–311.https://doi.org/10.5594/j18176.

[6] T. Toyama, K. Mishina, H. Tsuchiya, T. Ichikawa, H. Iwaki, Y. Gendai, H. Murakami, K. Takamiya, H. Shiroshita, Y. Muramatsu, and T. Furusawa, "A 17.7 Mpixel 120 fps CMOS image sensor with 34.8 Gb/s readout" in Proc. ISSCC Dig. Tech. Papers, Feb. 2011, pp. 420–422.

https://doi.org/10.1109/ISSCC.2011.5746379

[7] M. Furuta, Y. Nishikawa, T. Inoue, and S. Kawahito, "A high- speed, high-sensitivity digital CMOS image sensor with a global shutter and 12-bit column-parallel cyclic A/D converters," IEEE J. Solid-State Circuits, vol. 42, no. 4, pp. 766–774, Apr. 2007. 10.1109/JSSC.2007.891655

[8] J. H. Park, S. Aoyama, T. Watanabe, K. Isobe, and S. Kawahito, "A highspeed low noise CMOS image sensor with 13-b column- parallel singleended cyclic ADCs," IEEE Trans. Electron. Devices, vol. 56, no. 11, pp. 2414–2422, Nov. 2009. 10.1109/TED.2009.2030635

[9] Y. C. Chae, J. Cheon, S. Lim, M. Kwon, K. Yoo, W. Jung, D.-H. Lee, S. Ham, and G. Han, "A 2.1 M pixels, 120 frame/s CMOS image sensor with column-parallel ΔΣ ADC architecture," IEEE J. Solid-State Circuits, vol. 46, no. 1, pp. 236–247, Jan. 2011.

[10] 10.1109/JSSC.2010.2085910

[11] K. Kitamura, T. Watabe, Y. Sadanaga, T. Sawamoto, T. Kosugi, T. Akahori, T. Iida, K. Isobe, T. Watanabe, H. Shimamoto,H. Ohtake, S. Aoyama, S. Kawahito, and N. Egami, "A 33 Mpixel, 120 fps CMOS image sensor for UDTV application with two-stage column-parallel cyclic ADCs," in Proc. Int. Image Sens. Workshop, Jun. 2011, pp. 343–346.

[12] T. Watabe, K. Kitamura, T. Sawamoto, T. Kosugi, T. Akahori,T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, S. Aoyama, S. Kawahito, and N. Egami, "A 33 Mpixel 120 fps CMOS image sensor using 12b column-parallel pipelined cyclic ADCs," in Proc. ISSCC Dig. Tech. Papers, Feb. 2012, pp. 388–390

[13] 10.1109/ISSCC.2012.6177047

[14] S. H. Lewis, H. S. Fetterman, G. F. Gross, Jr., R. Ramachandran, and T. R. Viswanathan, "A 10-b 20-Msample/s analog-to-digital converter," IEEE J. Solid-State Circuits, vol. 27, no. 3, pp. 351–358, Mar. 1992 DOI: 10.1109/4.121557

[15] J. H. Park, S. Aoyama, T. Watanabe, T. Kosugi, Z. Liu, T. Akahori, M. Sasaki, K. Isobe, Y. Kaneko, K. Muramatsu, T. Iida, and S. Kawahito, "A high-speed low-noise CIS with 12b 2-stage pipelined cyclic ADCs," in Proc. Int. Image Sens. Workshop, Jun. 2011, pp. 339–342.

[16] K. Kitamura, T. Watabe, T. Sawamoto, T. Kosugi, T. Akahori,T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, S. Aoyama, S. Kawahito, N. Egami, "A 33-Megapixel 120-Frames- Per-Second 2.5-Watt CMOS Image Sensor With Column-Parallel Two-Stage Cyclic Analog-to-Digital Converters," IEEE Trans. Electron. Devices, VOL. 59, NO. 12, pp. 3426 - 3433 Dec. 2012

[17] DOI: 10.1109/TED.2012.2220364

[18] Snoeij, Theuwissen, Huijsing, "A low power coloumn parallel ADC for CMOS Imagers".

[19] Jun Liu "A Novel Small-Signal Model for Bulk FinFETs Accommodating Self-Heating Behaviors", Hangzhou Dianzi University, China, D. Hisamoto, W.-C. Lee, J. Kedzierski et al., "FinFET—a self- aligned double-gate MOSFET scalable to 20 nm," IEEE Trans- actions on Electron Devices, vol. 47, no. 12, pp. 2320–2325, 2000

[20] DOI: 10.1109/LED.2017.2707283

[21] D. Hisamoto, W.-C. Lee, J. Kedzierski et al., "FinFET—a self- aligned double-gate MOSFET scalable to 20 nm," IEEE Trans- actions on Electron Devices, vol. 47, no. 12, pp. 2320–2325, 2000

[22] DOI: 10.1109/16.887014

[23] B. Yu, L. Chang, S. Ahmed et al., "FinFET scaling to 10 nm gate length," in Proceedings of the IEEE International Devices Meeting (IEDM '02), pp. 251–254, San Francisco, Calif, USA, December, 2002

[24] DOI: 10.1109/IEDM.2002.1175825